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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,164	03/25/2004	Robert J. Schultz	RSTN-114	7766

30139 7590 03/09/2009

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2419	
MAIL DATE	**DELIVERY MODE**
03/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,164	SCHULTZ, ROBERT J.	
	Examiner	Art Unit	
	EUNSOOK CHOI	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17,18,20 and 21* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/1/2008 have been fully considered but they are not persuasive.

- Applicant argues on page 8 and 9 regarding claim 12 that the office action fails to explicitly assert that the cited references might teach "wherein the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit" and Rhoades does not teach a second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit. The examiner disagrees. Rhoades teaches in **Fig. 8, Perform Table Lookup** (a search of a first stage memory unit) is processed in parallel with **Transmission Error Detection – Packet Lifetime Calculations** (a second stage processing element, to allow a second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit). Rhoades teaches, further in detail, Fig. 14 table look up with internal/external RAM and [0083] adjacent PEs have close-coupled inter-processor communication paths that provide a low cost means of sharing and aggregating the results from individual PEs simultaneously with the parallel processing itself, as shown in Fig. 8 of Rhoades. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply Rhoades' table lookup with parallel packet processing, enabled

by [0064] the processor's hardware support for multithreading, to Key's arrayed processing engine in order to make efficient use of the processing power, bandwidth and high degree of concurrent operation (Paragraph 16, Rhoades).

- Applicant argues on page 11 regarding claim 1 that Rhoades does not teach performing search-independent processing using a second stage processing element in parallel with a first search. Rhoades teaches in **Fig. 8, Perform Table Lookup** (a first search) is processed in parallel with **Transmission Error Detection – Packet Lifetime Calculations** (a second stage processing element, performing search-independent processing using a second stage processing element in parallel with a first search).
- Applicant argues on page 11 regarding claims 6 and 18 that Rhoades does not teach the claim limitation that the office action relies on at least for similar reasons to those stated for claim 12. Refer to response to argument for claim 12 above.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) in view of Rhoades et al. (US 20030041163).

Regarding claim 12, Key teaches an array of processing elements **(Fig. 3 PEs)** having; at least one first stage processing element **(Fig. 3 the first PE 400)**; and

at least one second stage processing element **(Fig. 3 the second row PE 400)**; and a first stage memory unit **(Fig. 3 the first 330)** that is searched in response to search information from the first stage processing element. However, Key does not expressly teach the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet. **Rhoades** teaches in **Fig. 8, Perform Table Lookup** is processed in parallel with **Transmission Error Detection – Packet Lifetime Calculations**. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet in order to provide the optimal balance between the conflicting demands of speed and programmability (Paragraph 16, Rhoades).

4. Claims 1, 2, and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhoades et al. (US 20030041163) in view of Van Lunteren et al. (US Patent 7193997).

Regarding claim 1, Rhoades teaches performing a first search (**Fig. 8, Perform Table Lookup)** using a first stage processing element (**Fig. 8, Packet processing block, Determine Protocol-Initiate Lookup)** related to a packet using first search

information (**Fig. 8, Extract Lookup Key)**; performing, in parallel with the first search, search-independent processing using a second stage processing element (**Fig. 8, Packet processing block, Transmission Error Detection–Packet Lifetime Calculations)** on information related to the packet (**Fig. 8, Perform Table Lookup** is processed in parallel with **Transmission Error Detection–Packet Lifetime Calculations)**; and performing search-dependent processing using a result from the first search and a result of the search-independent processing **(Fig. 8, Process Lookup Result-Complete Tunneling Task)**. However, Rhoades does not teach producing second search information. Van Lunteren teaches in Fig. 10 parallel lookups are combined to produce search information. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to produce second search information in order to determine a plurality of predefined processing rules applies to a data packet (Col. 3 Lines 53-55, Van Lunteren).

Regarding claim 2, Rhoades and Van Lunteren teach the limitations for claim 1 as applied above. Van Lunteren teaches in Fig. 10 performing a second search using the second search information.

Regarding claim 3, Rhoades and Van Lunteren teach the limitations for claim 2 as applied above. Rhoades teaches in Fig. 8 the processors synchronize with ocher processors and hardware accelerators via semaphores (holding a processing state from the search-independent processing until the result from the first search is available).

5. Claims 6, 7, 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) in view of Rhoades et al. (US 20030041163) and Van Lunteren et al. (US Patent 7193997).

Regarding claim 6, Key teaches processing information related to a packet using a first stage processing element **(Fig. 3, the first PE 400)** to produce a first search key, wherein the first stage processing element is included within an array of processing elements; searching a first stage memory unit **(Fig. 3, the first 330)** using the first search key. However, Key does not teach performing, in parallel with the search of the first stage memory unit, search-independent processing on information related to the packet using a second stage processing element, wherein the second stage processing element is included within the array of processing elements; performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key; and searching a second stage memory unit using the second search key. Rhoades teaches the limitations as applied to claim 12 above.

However, Key and Rhoades do not teach to produce a second search key; and searching a second stage memory unit using the second search key. Van Lunteren teaches as applied to claim 1 above. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to produce second search information in order to determine a plurality of predefined processing rules applies to a data packet (Col. 3 Lines 53-55, Van Lunteren).

Regarding claim 7, Key, Rhoades, and Van Lunteren teach the limitations for claim 6 as applied above. Key teaches the limitations as applied to claim 3.

Regarding claim 11, Key, Rhoades, and Van Lunteren teach the limitations for claim 6 as applied above. Key teaches in Fig. 8 row synchronization logic 800 ensuring that each PE stage completes its processing of current context prior to loading new context at a new phase (forwarding information related to the packet to the second stage processing element before the result from the search of the first stage memory is produced).

Regarding claim 14, Key and Rhoades teach the limitations for claim 12 as applied above. However, Key does not expressly teach the second stage processing element is further configured to perform search-dependent processing using a result of the search of the first stage memory unit and a result from the search-independent processing to produce a search key. Van Lunteren teaches in Fig. 10 parallel lookups are combined to produce a search key. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the second stage processing element is further configured to perform search-dependent processing using a result of the search of the first stage memory unit and a result from the search-independent processing to produce a search key in order to determine a plurality of predefined processing rules applies to a data packet (Col. 3 Lines 53-55, Van Lunteren).

Regarding claim 15, Key, Rhoades, Van Lunteren teach the limitations for claim 14. Van Lunteren teaches in Fig. 10 a second stage memory unit that is associated with

the second stage processing element, wherein the search key is used to search the second stage memory unit.

6. Claims 13, 17, 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) in view of Rhoades et al. (US 20030041163) and Kaganoi et al. (US PGPUB 20030012198).

Regarding 18, Key teaches an array of processing elements **(Fig. 3 a programmable arrayed processing engine, 400)** having; a plurality of first stage processing elements **(Fig. 3, the first row of PEs)**; and a plurality of second stage processing elements **(Fig. 3, the second row of PEs)**; and a memory interface **(Fig. 3, 310)** that is configured to provide search information to a first stage memory unit from the plurality of first stage processing elements. However, Key does not teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements, the first and second stage processing elements are configured to allow the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit, where the searches are related to the same packets. Rhoades teaches the limitations as applied to claim 12 above. However, Key and Rhoades do not teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements. Kaganoi teaches in Fig.3 search results from CAM 13 and Associated Data Memory 15 are directly provided to the next processing stages. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide search results from the first stage memory unit directly to the

plurality of second stage processing elements in order to perform the retrieval processing without waste at all times (Paragraph 50, Kaganoi).

Regarding claims 13, Key and Rhoades teach the limitations for claim 12 as applied above. However, Key and Rhoades do not expressly teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements. Kaganoi teaches in Fig.3 search results from CAM 13 and Associated Data Memory 15 are directly provided to the next processing stages. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide search results from the first stage memory unit directly to the plurality of second stage processing elements in order to perform the retrieval processing without waste at all times (Paragraph 50, Kaganoi).

Regarding claim 17, Key and Rhoades teach the limitations for claim 12. Kaganoi teaches in Fig.3 first stage memory unit comprises content addressable memory.

Regarding claim 20, Key, Rhoades, and Kaganoi teach the limitations for claim 18 as applied above. Key teaches in Fig. 8 row synchronization logic 800 ensuring that each PE stage completes its processing of current context prior to loading new context at a new phase.

Regarding claim 21, Key, Rhoades, and Kaganoi teach the limitations for claim 18 as applied above. Key teaches in Fig. 3 330 - memory bus.

7. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhoades et al. modified by Van Lunteren et al. as applied to claim 2 above, and further in view of Khanna (US Patent 7219187).

Regarding claim 4, Rhoades and Van Lunteren teach the limitations for claim 2 as applied above. However, Rhoades and Van Lunteren do not teach producing a comparand and a mask as the second search information. Khanna teaches in Col. 2 Lines 10-19 the CAM device can be instructed by the processor to compare a search key, also referred to as a comparand (e.g., generated from packet header data), with data stored in its associative memory array. Khanna further teaches in Col. 9 Lines 31-62 global mask select circuit 607 selects the corresponding global mask ID (GMID 622) from search parameter table 525 in response to the activated GMSEL signal. The selected GMID is used to select a corresponding global mask GM(1) GM(z) from the global mask register 606 that globally masks the comparand data during a compare operation. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a comparand and a mask as the second search information in order for routers and CAM devices to perform the various lookups on packets (Col. 2 Lines 10-19 Khanna).

Regarding claim 5, Rhoades, Van Lunteren, and Khanna teach the limitations for claim 4. Khanna teaches in Fig. 6 and Col. 9 Lines 31-62 Block select circuit 605 outputs block select signal BSEL 609 that enables comparand drivers 608 to drive the comparand data into CAM block array 602 to participate in a compare operation if a stored CAM table ID for the CAM array 602 matches one of the CAM table IDs provided

from the search parameter table 525. The comparand data is globally masked by the selected global mask data by logically ANDing together the selected global mask data on a bit-for-bit basis with corresponding bits of the comparand data in the comparand drivers 608.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. modified by Rhoades and Van Lunteren et al. as applied to claim 6 above, and further in view of Khanna (US Patent 7219187).

Regarding claim 10, Key, Rhoades , and Van Lunteren teach the limitations for claim 6 as applied above. Khanna teaches the limitations as applied to claim 4 above. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a comparand and a mask as the second search information in order for routers and CAM devices to perform the various lookups on packets (Col. 2 Lines 10-19 Khanna).

9. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. modified by Rhoades and Van Lunteren et al. as applied to claims 6 and 7 above, and further in view of Kaganoi et al. (US PGPUB 20030012198).

Regarding claims 8 and 9, Key, Rhoades, and Van Lunteren teach the limitations for claims 6 and 7 as applied above. However, Key, Rhoades, and Van Lunteren do not expressly teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements. Kaganoi teaches in Fig.3 search results

from CAM 13 and Associated Data Memory 15 are directrly provided to the next processing stages. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide search results from the first stage memory unit directly to the plurality of second stage processing elements in order to perform the retrieval processing without waste at all times (Paragraph 50, Kaganoi).

Allowable Subject Matter

10. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to EUNSOOK CHOI whose telephone number is (571)270-1822. The examiner can normally be reached on Monday-Friday 8:00-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC
3/3/2009

/Wing F. Chan/
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3/5/09